A Methodology for the Design of Capacitive Feedback LNAs based on the gm/ID Characteristic

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***Abstract*—This paper presents a g_m/I_D based design methodology for a capacitive feedback LNA topology. The proposed method gives the optimal value of g_m/I_D to achieve the required performances (Gain and Noise Figure) while ensuring the minimum consumption. Moreover, it makes possible the sizing of all the components of the structure with a degree of freedom for the inductance value needed for the input power matching. This methodology is illustrated through the design of a 2.4GHz LNA in the 28nm FDSOI technology from ST-Microelectronics.**

Keywords—LNA; capacitive feedback; low power; g_m/I_D; 28nm FDSOI

I. INTRODUCTION

Cost reduction and power saving are fundamental requirements in mobile RF applications. The cost of devices such as LNAs is mainly due to the number and the size of inductors used in the design. Unfortunately, advanced technologies do not directly impact the size of such devices. However, in advanced CMOS technologies, power consumption can be reduced thanks to the performance enhancement in the frequency transition (f_t). For such technologies, recent works show that good trade-offs between performances and consumption can be obtained in moderate or weak inversion region [1]. In this context, different figures of merit such as $g_m.f_T/I_D$ [2] and g_m^2/I_D [3] or the inversion coefficient [4] have been explored to determine the best region of operation in RF design. These studies are useful to identify the best region of operation to optimize a given FoM but do not give a method for the sizing of all components. In this paper we present a complete method to size capacitive feedback LNAs. This topology is chosen for its compactness since only one inductor is used (in the input matching network). The presented design flow allows reaching some given performances (Noise Figure *NF* and voltage gain G_{lna}) with the minimum power consumption while having a design constraint on the value of the inductor to better control the cost of the LNA . With the same philosophy of methods developed in the early nineties to design OTA [7], our procedure is based on a g_m/I_D approach which is suitable for RF design in advanced technologies such as FDSOI or FinFET. This method allows the sizing of all the components to reach a given NF and voltage gain while maximizing the g_m/I_D to minimize the power consumption. In addition, even if the linearity is not considered as a design constraint, this method leads to good IIP3 performances because it tends to reduce the input quality factor which causes high non-linearity.

Acknowledgement: this work has been granted by the European Community through the projects THINGS2DO and CONVERGEANCE.

II. LNA DESIGN

A. Method overview

In advanced technologies, the use of regional based analytical model to size a topology is less and less accurate especially in a low power context where weak or moderate inversion is needed to reduce the power consumption. This leads to an extensive use of simulations with numerous iterations to obtain the desired requirements. Hence, a g_m/I_D based method is a way of reducing these iterations. g_m/I_D methodologies are based on a simple characterization (as depicted in Fig. 1(a) of the transistor in all region of operation and can help the designers to optimize the power efficiency with respect to a given requirement. As shown in [7], an OTA has been designed by using the g_m/I_D methodology. As depicted on Fig. 1(b), the designer uses a set of equations to determine the g_m/I_D value needed to reach requirements. Then, based on model parameter extractions that give, as a function of g_m/I_D, design parameters such as f_t, V_{gs} or r_{ds} and the normalized current $I_D/(W/L)$, the topology can be sized.

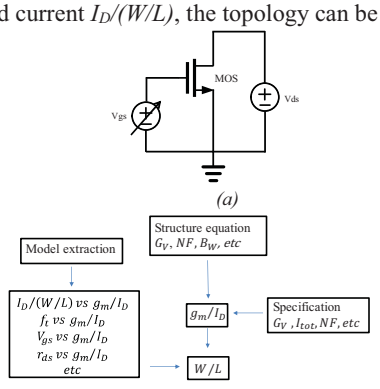

Fig. 1 (a) Extraction of the MOS transistor and (b) Method principle

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B. LNA Input matching

The studied topology is shown in Fig. 2(a) with its small signal equivalent circuit in Fig. 2(b).

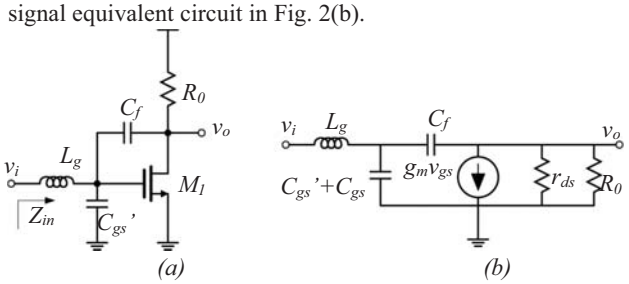

Fig. 2 (a) Capacitive Feedback LNA structure and (b) its equivalent small signal model

The input impedance of the structure is given in (1).

$$Z_{in} = L_g p + \frac{1}{C_{gs} p} // Z_M \tag{1}$$

with L_g the input inductance, C_{gs} the input parasitic capacitances of the transistor M_1, and Z_M the Miller impedance due to the capacitive feedback which can be expressed as follow if $C_f \omega \ll g_m$:

$$Z_M = \frac{1}{C_f p (1 - G_v)} \quad \text{with} \quad G_v = \frac{v_o}{v_{gs}} = \frac{R_L (C_f p - g_m)}{1 + R_L C_f p} \approx -g_m R_L \tag{2}$$

with $R_L = r_{ds} // R_0$. With Z_M, it is possible to express the real part of Z_{in} as follow:

$$Z_M \approx \frac{1}{C_f p (1 + g_m R_L)} + \frac{R_L}{(1 + g_m R_L)} = \frac{1}{C_M p} + R_M \tag{3}$$

So the real part can be written:

$$\Re(Z_{in}) = R_M \frac{1 + Q_s^2}{1 + Q_e^2} \approx \frac{1 + Q_s^2}{1 + Q_e^2} \frac{R_L}{(1 + g_m R_L)} \tag{4}$$

$$\Im m(Z_{in}) = L_g p + \frac{Q_e^2}{(C_s + C_{gs} + C_p) p (1 + Q_e^2)} \tag{5}$$

$$with\ Q_s = \frac{1}{R_M C_M \omega} = \frac{1}{C_f R_L \omega}\ and\ Q_e = Q_s \left(1 + \frac{C_{gs} + C'_{gs}}{C_f} \frac{1 + \frac{1}{Q_s^2}}{(1 + g_m R_L)} \right)$$

The bandwidth of a capacitive feedback topology is highly limited by C_f and can be expressed as follow if we neglect C_{ds} and C_{db}:

$$Bw \approx \frac{1}{2\pi R_L C_f} = \frac{Q_s \omega_0}{2\pi} \tag{6}$$

Then, the gain, the real part of the input impedance and the bandwidth can be chosen independently if a capacitor C'_{gs} is added in parallel with C_{gs}.

In a conventional approach, the transconductance g_m would be set in agreement with the noise figure since it dominates the noise performance as it is shown in the next section, R_L would be determined to achieve a given gain, C_f would be set to ensure a given bandwidth, then C'_{gs} would be used to obtain a 50Ω input resistance. L_g would be used to cancel the input imaginary part. Considering L_g as a design variable sized to cancel the imaginary part of Z_{in} can have a dramatic impact on the size of the circuit. We propose here to control the value of L_g through the input Q-factor Q_e and to set it at the beginning of the sizing.

$$Q_e = \frac{L_g \omega_0}{R_g} \tag{7}$$

If L_g is set, C_f and C_{gs}' are needed to synthesize the 50Ω input impedance and the bandwidth is no more a design variable. As a consequence, few iterations could occur in the method. In addition, we can notice that low values of L_g reduce Q_e and limit the overall voltage gain. However, low Q_e limits the value of v_{gs} which helps reducing the Non-Linearity.

C. $g_m.r_{ds}$ versus g_m/I_D

In this method, we propose to minimize the power consumption to achieve a given intrinsic gain ($g_m.r_{ds}$) while targeting a given NF. In this context, the optimal value of g_m/I_D is determined based on the technology capability (intrinsic gain of the transistor) and the gain of the capacitive feedback topology which is given by (8). For the frequencies above the cutting frequency imposed by C_f, the voltage gain is:

$$G_{\ln a} = \frac{V_o}{V_i} = g_m * (r_{ds} // R_0) * \sqrt{1 + Q_e^2} \tag{8}$$

From (8) it is possible to express the gain as a function of the drain source voltage of the transistor (V_{ds}) and the Early voltage (V_{ea}) which can be considered as a constant in a first order approximation.

$$G_{\ln a} = \frac{g_m}{I_D} \sqrt{1 + Q_e^2} \left(\frac{(V_{DD} - V_{ds})(V_{ea} + V_{ds})}{V_{DD} + V_{ea}} \right) \tag{9}$$

The gain is maximum for $V_{ds}=(V_{DD}-V_{ea})/2$ where $r_{ds}=R_0$ and the MOS should be biased at this value, otherwise it should be biased closed to the saturation voltage (V_{dsat}) and in this case $r_{ds}>R_0$. In advanced technologies, V_{ea} is small and is often lower than V_{DD}.

From (8) it is possible to write the intrinsic gain ($g_m.r_{ds}$) as a function of g_m/I_D for a given V_{ds} :

$$\frac{1}{g_m r_{ds}} = \frac{\sqrt{1 + Q_e^2}}{G_{\ln a}} - \frac{1}{\frac{g_m}{I_D}(V_{DD} - V_{ds})} \tag{10}$$

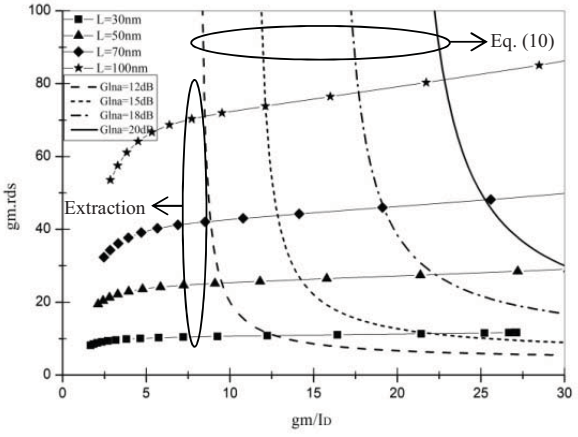

Fig. 3 $g_m.r_{ds}$ *vs* g_m/I_D for Q_e =1 and $V_{ds}=(V_{DD}-V_{ea})/2$

Equation (10) is plotted in Fig. 3 (dashed curves) for different values of G_{lna}, Q_e=1 and V_{ds} =(V_{DD}-V_{ea})/2. It shows the dependence of the intrinsic gain with the g_m/I_D value. Moreover, the intrinsic gain is technologically dependent on the ratio g_m/I_D. It is then possible to draw the transistor intrinsic gain behaviour as a function of g_m/I_D for a given technology as in Fig. 3 (plain curves) for the FDSOI 28nm technology from ST-Microelectronics and for different gates length L. Plotting these two relationships on the same graph allows finding an operating point that maximises g_m/I_D and then optimise the power consumption for a given gain and a given technology. We can observe that using small gate length increases the g_m/I_D for a given gain which helps reducing the power consumption for a given g_m.

D. NF versus g_m

The purpose of this method is to control the value of the *NF*. For a capacitive feedback topology, the *NF* is calculated as follow if we neglect the inductor L_g at the input (Q_e=0):

$$NF = 1 + \frac{\gamma g_m \left(1+\left(R_g C_f \omega_0\right)^2\right)}{R_g\left(g_m{}^2+\left(C_f\omega_0\right)^2\right)} + \frac{\left(1+\left(R_g C_f \omega_0\right)^2\right)}{R_g R_L\left(g_m{}^2+\left(C_f\omega_0\right)^2\right)} \quad (11)$$

$$\approx 1 + \frac{\gamma}{g_m R_g} + \frac{1}{g_m{}^2 R_g R_L} \quad (12)$$

where R_g is the source impedance and γ is the noise excess factor which can be extracted for a given technology as shown in Fig. 4 for the FDSOI 28nm. Hence, it is possible to determine the value of g_m needed to achieve a maximum noise factor with no consideration on the load and the size of the transistor.

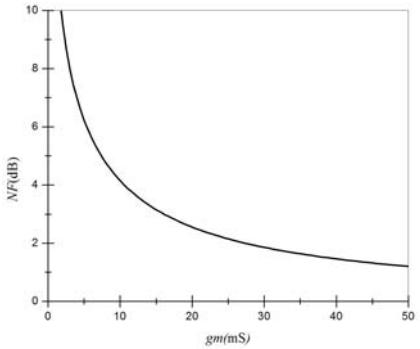

Fig. 4 NF vs gm/I_D

E. Transistor Sizing

The size (width) of the transistor depends on the g_m/I_D and the drain current density through the intrinsic relationship $I_D/(W/L)$ *vs* (g_m/I_D) which can be extracted for a given technology [7]. This relationship is shown in Fig. 5. The biasing (V_{gs}) of the MOS also depend on g_m/I_D for a given size and can be obtained after extraction of the relationship of V_{gs} *vs* g_m/I_D once the size is known.

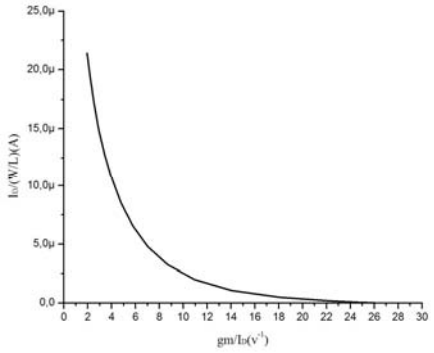

Fig. 5 I_D/(W/L) vs gm/I_D

The C_{gd} and C_{gs} capacitors highly depend on the size of the transistor and the values of C_f and C_{gs}' added for impedance matching can then be determined after sizing the transistor.

F. Method summary:

The principle of the proposed design method is shown in Fig. 6:

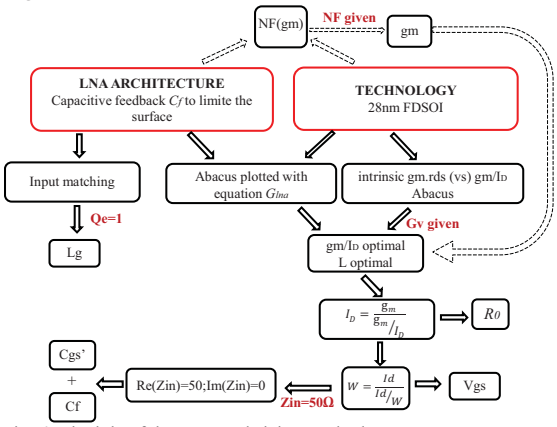

Fig. 6 Principle of the proposed sizing method

1. G_{lna}, *NF* and L_g are set regarding the application needs.
2. V_{ea} is extracted and V_{ds} is set to (V_{DD}-V_{ea})/2
3. Optimum g_m/I_D and L are determined tanks to the $g_m.r_{ds}(g_m/I_D)$ characteristics (Fig. 3)
4. Based on the maximum *NF* value, the transconductance g_m is set with (12).
5. The current I_D is determined from g_m and g_m/I_D and the load R_0 is determined so that V_{ds} =(V_{DD}-V_{ea})/2.
6. The width W of the transistor M_1 is set with $I_D/(W/L)$ *vs* (g_m/I_D) (Fig. 5), and the gate voltage bias can then be determined to achieve the needed current.
7. C_f and C_{gs}' are calculated to simultaneously have Im(Z_{in})=0 and Re(Z_{in})=50Ω.

III. POST-LAYOUT SIMULATION RESULTS

Fig. 7 shows the complete circuit with the component dimensions for G_{lna} =15.7dB and L_g=3.8nH. The results of post-layout simulation are shown in TABLE 2.

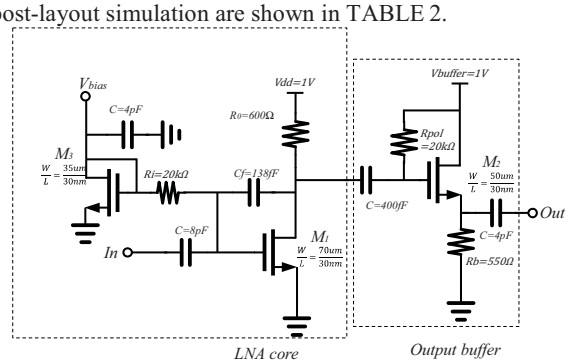

Fig. 7 Implemented circuit

The method is applied to a 28nm FDSOI technology from ST-Microelectronics. A maximum NF of 3dB is targeted at 2.4GHz for G_{lna} =15; 18 and 20 dB. Q_e is chosen to be equal to one which gives with (7) a value of L_g=3.8nH. Such inductor value can be integrated or synthesized in the input bounding. TABLE 1 shows the main design parameters obtained theoretically from step 3 to step 6. The design kit is used to evaluate the different parameters of the transistor as a function of g_m/I_D (Fig. 3, Fig. 4 and Fig. 5), and by considering an inductor synthesized by a bonding wire. High gain maximizes the g_m/i_D which gives, for a quite constant g_m, lower power consumption and lower f_T.

TABLE 1 LNA PERFORMANCES OF DIFFERENT GM VALUES

G_{lna} (dB)	NF (dB)	g_m (mS)	g_m/I_D (V^{-1})	L (nm)	I_D (mA)	R_0 (Ω)	W (µm)	f_t (GHz)
15	<3	15	22	30	0.681	734	43	52.6
18		14	22.5	50	0.622	803	37.6	40
20		12	25	70	0.48	1041	32	31.3

Three LNA have been designed based on these initial parameters. Input matching has been obtained by adding C_f and $C_{gs'}$ (step 7). The final RF performances after slight tuning are given in TABLE 2. Overall performances of LNAs are compared with the following FoM :

$$FoM = 20\log_{10}\left(\frac{G_{V\,av.[lin]}\,BW_{[GHz]}\,IIP3_{[mW]}}{P_{dc[mW]}\left(F_{av.[lin]}-1\right)}\right) \qquad (13)$$

These performances are comparable with the state of the art. The power consumption is lower than 1mW and the IIP3 lower than -5dBm.

IV. CONCLUSION

Based on the proposed methodology, three designs have been realized. Thanks to our method, a capacitive feedback LNA can be sized to reach given G_{lna}, NF and L_g values at minimum power consumption. The g_m/I_D approach appears to be well suited for advanced technologies for which the f_t is very high and doesn't limit the performances.

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TABLE 2 COMPARISONS PERFORMANCES OF LNA

	Tech (nm)	G_{lna} (dB)	NF (dB)	S_{11} (dB)	IIP3 (dBm)	P. Cons (mW)	BW (GHz)	V_{DD} (V)	L_g (nH)	FoM
[1]	65 CMOS	8.7	3.74	-22	n/a	0.315	-	0.7	19.6+2.3+18	-
[6]	90 CMOS	12.6	5.5-6.5	<-10	-6~-9	7	6.9	0.5	3.1+3.1	6
[5]	90 COMS	9.7	4.36	<-10	-4	0.684	0.8	1.2	0.75+11.1+10.5	8.1
[8]	130 CMOS	12.3	4.9-6	<-10	-11.5~-9.5	0.4	2.2	1	0	0.7
[9]	65 CMOS	21.2	2.8-4	-<-10	-7.7	2	4.3	1.2	1.5	9.25
This work	28 FDSOI (post-layout simulation)	15.7	3	-17.8	-6.75	0.76	3	1	3.8	16.7
		18.3	2.57	-20.7	-7.2	0.628	2.7			20
		19.8	2.6	-17.4	-8.5	0.55	3.4			21.68